Digital Verification Designer

JOB PURPOSE:

This position is for PHY transceiver digital blocks level and chip level verification.

JOB DUTIES AND RESPONSIBILITIES:

- Develop verification test plans and test cases that cover all system features of complex chip
- Writing/debugging test code/ test benches
- Work closely with the design team to ensure timely delivery and quality designs.

QUALIFICATIONS/SKILLS:

- **Specialized skills**
    - Experience with expertise in the latest design verification methodology such as UVM, assertion based coverage driven verification, and Objected Oriented Programming.
    - Experience with expertise in the chip level verification environments setup, code/function coverage collection, gate-level verification setup.
    - Proficient with modern design verification tools and languages (e.g. SystemVerilog, SVA, C++/SystemC, Perl, Unix Shell script)
    - Expertise in verifying complex designs at SOC/chip and block levels.
    - In depth knowledge of digital logic design and ASIC COT design flow.
    - Strong debugging and problem solving skills.

- **Education requirements**

  BS/MS (preferred) in EE or CS

- **Experience requirements**

  5+ working experience in the field of digital verification.

- **Attributes/Aptitudes/Attitudes**
    - Ability to work well in a fast-paced engineer group
    - Flexible in terms of working hours