Job Description

Job Title	**Digital Verification Engineer**
Location	**San Diego, CA**
Manager	**Director, Technical Design Engineering**

JOB PURPOSE:

This position is for PHY transceiver digital blocks level and chip level verification.

ESSENTIAL FUNCTIONS:

- Develop verification test plans and test cases that cover all system features of complex chip
- Writing/debugging test code/ test benches.
- Work closely with the design team to ensure timely delivery and quality designs.

QUALIFICATIONS/SKILLS:

- Experience with expertise in the latest design verification methodology such as UVM, assertion based coverage driven verification, and Objected Oriented Programming.
- Experience with expertise in the chip level verification environments setup, code/function coverage collection, gate-level verification setup.
- Proficient with modern design verification tools and languages (e.g. SystemVerilog, SVA, C++/SystemC, Perl, Unix Shell script)
- Expertise in verifying complex designs at SOC/chip and block levels.
- In depth knowledge of digital logic design and ASIC COT design flow.
- Strong debugging and problem solving skills.

EDUCATION/EXPERIENCE

- BS/MS(preferred) in EE or CS
- 5+ working experience in the field of digital verification.

ATTRIBUTES/APTITUDES/ATTITUDE

- Thrives in a highly collaborative and dynamic work environment
- Possesses a quality-oriented mindset and attention to details
- Demonstrate superb communication skills
- Strong inner drive and self-motivation
- Creativity in problem-solving